Philip W. Mason, Ph.D.

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Summary

An experienced goal-oriented, reliability engineering professional with a background in semiconductor design for reliability, product reliability, customer technical support, and reliability during technology development. Strong analytical and organizational skills with the ability to diagnose highly technical problems and develop innovative solutions.

Professional Experience

Member of Technical Staff level 2
Qorvo Inc., (formerly RFMD)
Greensboro, NC 2007-2020

- Determined Si antenna tuner RF reliability stress degradation modes at the transistor-level (snapback and gate oxide), and where to place limits to maximize performance while ensuring field reliability.
- Helped design RF reliability test systems for antenna tuners for measuring both large-signal electrical and thermal performance.
- Gave routine presentations to large world-wide cell phone manufacturer about reliability topics for antenna tuner products.
- Identified and modeled RF harmonic source from the SOI silicon substrate and how it impacts device RF performance, especially due to intrinsic carriers at high temperatures.
- Determined SiGe RF PA's limiting reliability degradation mode of base electromigration, for in-house unit cell. Gave, to both unit-cell and product designers, recommendations and generated calculators about tradeoffs between current, temperature, and reliability.
- Assembled and led cross-organizational teams for reliability evaluations.
- Mentored two new hires for 2 years each

Distinguished Member of Technical Staff
LSI Corporation (formerly Agere Systems/Lucent Technologies Bell Laboratories)
Allentown, PA 2002-2007

- Technology Development, Transfer, Evaluation: Silicon Reliability
- Performed reliability assessments and gave recommendations regarding large-volume IC products for various end-customer needs including tailoring voltage levels, operational temperatures, design mistake risk assessment, and field returns.
- Managed reliability test lab and performed device characterization measurements on wafers and packages.
- Interfaced with external foundries for evaluating and qualifying their CMOS device-level technology reliability for use in products.
- Developed reliability requirements and projection models for gate oxides, nMOS and pMOS transistor reliabilities for 65nm, 90nm, 0.13um and older technologies.
- Coordinated transfer of reliability test lab from Orlando to Allentown in 2002

Member of Technical Staff
Bell Labs, Lucent Technologies, Orlando, FL 1997-2002
Technology Development: Silicon Reliability

- Collaborated with Bell Labs Research to develop methodologies, test structures and degradation models for assessing plasma damage impact to electronic devices and product yield and reliability.
- Developed methodologies, test structures, and degradation models for developing transistor ultra-thin gate oxides of advanced IC technologies.
- Drove charging damage evaluation of CMOS technologies during development.
- Worked with design organizations to implement methodologies to ensure charging damage did not impact IC yield and reliability.

Education
- Ph.D. in Physics: Lehigh University, Bethlehem, PA, 1998
- Dissertation: An Optical and Magnetic Resonance Study of Point Defects in Silicon, Diamond, and Aluminum Nitride
  - M.S. in Physics: Lehigh University, Bethlehem, PA 1993
  - B.S. in Physics: Worcester Polytechnic Institute, Worcester, MA, 1991

Professional Associations
- Sigma Xi: 1993 to present
- IEEE: full member 2006-present

Publications

A Methodology for Accurate Assessment of Soft-broken Gate Oxide Leakage and the Reliability of VLSI Circuits, Mason, P.W, et al., 2004 42nd International Reliability Physics Symposium Proceedings, pg. 406.
Relationship between yield and reliability impact of plasma damage to gate oxide, P.W. Mason, D.K. DeBusk, J.K. McDaniel, A. S. Oates, K. P. Cheung, Proc. of the 2000 Plasma and Process Induced Damage Symposium, pp. 2 (2000).
Quantitative Yield and Reliability Projection from Antenna Test Results - A Case Study, P. W. Mason, K.P. Cheung, D.K. Hwang, et al., Proc. of the 2000 Symposium on VLSI Technology, pp. 96 (2000).

Patents:

April, 2002, US Patent #6,365,426: A Methodology for Evaluating the Impact of Plasma Damage to Integrated Chip Yield and Reliability
June 2007, US patent: A Methodology for Assessing the Impact of Multiple Soft-breakdowns on Integrated Circuitry and Products.

Presentations:
- Invited Presentation, Microelectronics Reliability and Qualification Workshop 2005, Strategy for Providing Customers a Rapid Product-Level Reliability Qualification Using Advanced Foundry Technologies
- Plasma Process Induced Damage 2003: ½ day tutorial presented: An Overview of the Charging Damage Impact on Advanced Integrated Circuit Reliability.

Review committees:
- Reviewer for Transactions on Device Materials and Reliability 2003-2016
- Reviewer for Electron Device Letters 2001-2003